Notes on 2020.1 Vivado HLS Tutorial – Chapter 7 28/06/2022

Completing Chapter 7 should take you 1 – 1.5 hours if you have completed the previously suggested tutorial exercises.

Ch. 7 uses a small matrix multiplication example to discuss several optimization approaches. To achieve optimality and surpass a single cycle latency per input, array reshaping and code restructuring are used to implement a streaming solution that uses FIFO data interfaces.

Specific notes follow:

- Modify the following line of the `run_hls.tcl` script **for both labs** before you begin them:

  ```
  set_part {xc7z020clg484-1}
  ```

  This will affect the absolute values for some results, but the trends will be like those described in the tutorial documentation.
- It is worth noting the comment after step 9 at the bottom of page 143.
- The reason given at the end of the third line from the top of page 145 for not achieving an II of one is incorrect. The reason for the delay in the 2nd read is because there is a read after write (RAW) hazard on `res[i][j]`.
- It is worth noting the comment in the last paragraph of page 147.
- The data reported in Figure 7-13 differs for the xc7z020 device – it should be as illustrated below:

Target device: xc7z020-clg484-1

Performance Estimates

Timing

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	13.33 ns	9.512 ns	1.67 ns

Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		
min	max	min	max	min	max	Type
12	12	0.160 us	0.160 us	12	12	none

Detail

Instance

Loop

	Latency (cycles)			Initiation Interval			
Loop Name	min	max	Iteration Latency	achieved	target	Trip Count	Pipelined
- Row_Col	10	10	3	1	1	9	yes

- Some of the statistics reported below Figure 7-13 on page 150 should be updated for the xc7z020 device. In particular, the loop latency is 9+3-1 cycles to complete, but

Vivado reports 10 as it does not count the last output cycle. The overall task latency is 1+10+1 cycles since one cycle is required to enter and one to exit the loop.

- The values in Figure 7-19 differ slightly for the xc7z020 device.
- It is worth noting the comments contained in the two paragraphs on pipelining before Lab 2 is introduced on page 155.
- Do not worry about Steps 6 and 7 of Lab 2 on page 157.