Notes and questions on 2020.1 Vivado HLS Tutorial – Chapter 4 Revised 9/05/2022

Completing Labs 1-3 and Steps 1-2 of Lab 4 of Chapter 4 should take about 2 hours assuming you have set up your lab environment and have completed the previously suggested tutorial exercises.

Ch. 4 covers some basic information about the types of interfaces you can use to communicate with your HLS generated core. Lab 3 and Steps 1-2 of Lab 4 reward you with a greater appreciation for the productivity HLS affords in terms of exploring hardware design alternatives and optimizing for both speed and area.

Specific notes follow:

- Since WebPack does not support the range of devices used in the tutorial, choose the **ZedBoard** "board" or the **xc7z020clg484-1** "device" as the "part" for all your projects. You will need to edit [`run_hls|script].tcl` scripts that use any other devices to avoid project set-up and compile time errors.
- You will need to comment out the directive `#pragma HLS INTERFACE ap_ctrl_none port=return` at line 49 in `adders.c` in Step 2 of Lab 1 to obtain the output depicted in Figure 4-4.
- Before commencing Step 2 of Lab 3, hold down the **Ctrl** key and click on line 46 of `array_io.c` to open `array_io.h`
- Before commencing the sub-steps of Lab 3, Step 3, click on the Analysis perspective and confirm that you understand the loop execution schedule for `solution1` as explained at the top of page 76.
- At the end of Lab3, Step 3 examine the loop execution schedule in the Analysis perspective. Can you explain the observed schedule?
- Before commencing Step 5 of Lab 3, examine the loop execution schedule in the Analysis perspective. Can you explain the observed schedule?
- Figure 4-29 compares the resource utilization estimates for the 4 solutions to Lab 3. Why do the resources used decrease as latency decreases?
- Figure 4-32 relates to a superseded version of the tool – both **axis** interface directives include the words "`register both`" by default, in 2020.1
- **Do not proceed past Lab4, Step 2**